High Precision Performance Measurement of Network Device

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1 Introduction

In relation with tremendous increase of Internet users, amount of data transmitted on Internet and network devices used by Internet Service Providers (ISP) explosively increased. In such an era, it is a matter of cause that engineers of ISPs and online service operators wish to measure performance of their network devices. However, in order to carry out high precision performance measurement of network devices, possession of special hardware testers are required. Reasons behind this are that, with software implementation carried on on OS and Personal Computer(PC), network adapters' queuing systems, buffering systems, and interrupt t timing, PC's memory, CPU and I/O buses, and even the measurement implementation itself presents dynamics and distortions with the result of measurement, which makes the result imprecise [1]. On the other hand, network measurement hardware tools are implemented with ASIC and printed circuits, making their designs and functions virtually impossible to be modified after shipments and they are very expensive and poory versatile[2]. In recent years, Field Programmable Gateway Alley (FPGA), a Large Scale Integrated-circuit (LSI) where its internal logic can be modified, are being noted in the field of computer engineering. This is because, it can function on high speed clocks such as 128MHz and its internal logic can be changed for large number of times.

2 The research's goal and requirement

This research is aimed at achieving high precision measurement of network devices with FPGA, which cannot be implemented with software. Besides that, this research will follow the guideline of RFC2544[3] and carry out measurement of network devices' internal delay and drop rate of Ethernet frame at maximum ethernet transmission rate with number of different Ethernet frame sizes. Target of the measurement in this research will be limited to network devices that supports Gigabit Ethernet, defined in IEEE 802.3ab[4].

3 Approach

Therefore the implementation in the research will be put into practice on NetFPGA, which is a PCI card with 4 Gigabit Ethernet interfaces and FPGA. In the implementation, two of the NetFPGA's Gigabit Ethernet interfaces are connected to Device Under Test (DUT). Ethernet frames, with time-stamps sent embedded, are sent from one of the interfaces and receive the Ethernet frames with the another interface. After that, calculate the time taken for each ethernet frames to be sent back to the implementation from DUT, by subtracting time-stamp at received timing and time-stamp embedded, and send the data to the PC through PCI bus.

4 Verification condition

In order to carry out high precision measurement, delay generated by the implementation and the implementation's accuracy must be evaluated. In this research, two verification conditions are presumed.

image 1: condition 1

In the verification condition one, shown on the image 1, implementation is performed on the NetFPGA and the Gigabit Ethernet interfaces for measurement are connected through with a short UTP cable. After that, delay measurement will be carried on, in order to measure the delay generated by the implementation and check that there is no irregularity in data from measurement.

image 2: condition 2

On the verification condition 2, shown on the image 2, delay measurement will be carried on with an UTP cable, which is drastically longer the one used on the condition 2, will be used. Subtract data retrieved from the measurement by data measured from the condition 1 and compare the result with the theoretical value, derived from difference in cable lengths, to see if there is no great deviation and prove the implementation's accuracy.

5 CONCLUSIONS

Through this research, network devices' performance will be tested with high precision, using numbers of ether frames with varying sizes and protocols with FPGA. This is in order to clarify network devices' performance and problems, which could not be elucidated by software.

6. REFERENCES

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